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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,300	01/17/2002	Vishnu K. Agarwal	303.780US1	5007

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EXAMINER	
PHAM, HOAI V	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/053,300	AGARWAL ET AL.	
	Examiner	Art Unit	
	Hoai v. Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2005* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-28 and 58-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-28 and 58-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *06/17/05* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-7 and 9-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chern [U.S. Pat. 6,287,921] IDS, in view of Ho et al. [U.S. Pat. 5,674, 775] IDS.

With respect to claims 1-3, 6, 7, 9, 10, 15-18, 21, 24, 26 and 28, Chern (figs. 2-3, col. 3) discloses transistor structure having reduced transistor leakage attributes, comprising:

a p-type substrate (10) having at least one trench wall (40);

an oxide layer (20) (see fig. 2 and col. 3, lines 16-18);

a nitride layer (30) (see fig. 2 and col. 3, lines 16-18) wherein the oxide layer, the nitride layer and a portion of the substrate form a process stack, the oxide and nitride layers being a pull back distance in a range from about $25A^0$ to about $300A^0$ from the trench wall thereby forming an exposed implant region (50A) (see fig. 3 and col. 3, lines 42-52);

a p-type dopant (70) in the implant region having the same type as the substrate type (see fig. 3 and col. 3, lines 11-13) where by the threshold voltage in the implant region is approximately equal to or greater than the threshold voltage on the portion of the substrate and whereby the pull back distance defines a width of the implant region which is approximately uniform around the process stack; and

a third layer (80) forming a plug in a shallow trench isolation of the substrate (see fig. 4 and col. 4, lines 1-5). It is noted that, the dopant concentration at the edging regions 50A is much heavier than that at the central area of the substrate underneath the oxide layer (20). Therefore, the threshold voltage at the edging regions 50A is greater than the threshold voltage at the central area of the substrate underneath the oxide layer (20).

Chern substantially discloses all the limitation as claimed above except a corner surface of the trench wall having a round contour. Ho et al. discloses a corner surface (28) of the trench wall having a round contour (see fig. 4 and col. 4, lines 45-46). Therefore, it would have been obvious to the skilled in the art at the time the invention was made to form the corner surface of the trench wall having a round contour as

taught by Ho et al. into the device of Chern in order to prevent parasitic field FET's and improve the isolation capabilities of the trench (see col. 5, lines 12-15).

With respect to claims 4, Chern does not disclose the exact concentration, as claimed by Applicant. However, the concentration range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

With respect to claims 5, 13 and 14, Chern disclose that the dopant has an implant energy from about 5 to about 25 KeV or less than or equal to about 10 KeV (see col. 3, lines 55-58).

With respect to claim 11, Chern disclose an N-type substrate (see col. 4, lines 49-51) and an N-type dopant (see col. 5, lines 24-28).

With respect to claims 12 and 25, Chern disclose that the dopant is one of Boron and BF (see col. 3, lines 55-57).

With respect to claim 19, Chern disclose that the dopant is present in the substrate at the at least one trench wall (see fig. 3).

With respect to claim 20, Chern disclose that the at least one trench wall is angled in relation to the surface (see fig. 3).

With respect to claims 22-23 and 27,Chern disclose that the implant region (50A) occupies a mirgration region adjacent to the oxide layer (20) (see fig. 3).

4. Claims 58-77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chern [U.S. Pat. 6,287,921] IDS, and Ho et al. [U.S. Pat. 5,674, 775] IDS, in view of Salling et al. [U.S. Pat. 6,515,889].

With respect to claims 58-65, 67, 72-75 and 77, Chern (figs. 2-3, col. 3) discloses transistor structure having reduced transistor leakage attributes, comprising:

a p-type substrate (10) having at least one trench wall (40);

an oxide layer (20) (see fig. 2 and col. 3, lines 16-18);

a nitride layer (30) (see fig. 2 and col. 3, lines 16-18) wherein the oxide layer, the nitride layer and a portion of the substrate form a process stack, the oxide and nitride layers being a pull back distance in a range from about $25A^0$ to about $300A^0$ from the

trench wall thereby forming an exposed implant region (50A) (see fig. 3 and col. 3, lines 42-52);

a p-type dopant (70) in the implant region having the same type as the substrate type (see fig. 3 and col. 3, lines 11-13) where by the threshold voltage in the implant region is approximately equal to or greater than the threshold voltage on the portion of the substrate and whereby the pull back distance defines a width of the implant region which is approximately uniform around the process stack; and

a third layer (80) forming a plug in a shallow trench isolation of the substrate (see fig. 4 and col. 4, lines 1-5). It is noted that, the dopant concentration at the edging regions 50A is much heavier than that at the central area of the substrate underneath the oxide layer (20). Therefore, the threshold voltage at the edging regions 50A is greater than the threshold voltage at the central area of the substrate underneath the oxide layer (20).

Chern does not disclose a corner surface of the trench wall having a round contour. Ho et al. discloses a corner surface (28) of the trench wall having a round contour (see fig. 4 and col. 4, lines 45-46). Therefore, it would have been obvious to the skilled in the art at the time the invention was made to form the corner surface of the trench wall having a round contour as taught by Ho et al. into the device of Chern in order to prevent parasitic field FET's and improve the isolation capabilities of the trench (see col. 5, lines 12-15).

Chern does not mention that the shallow trench isolation is used in an electronic system. However, Salling et al. discloses that the shallow trench isolation (105) is used

in an electronic system (see fig. 10 and col. 11, lines 56-61). Therefore, it would have been obvious to one having skilled in the art at the time the invention was made to use the shallow trench isolation is used in an electronic system as taught by Salling et al. in order to prevent leakage current entering the active device.

With respect to claim 66, Chern disclose an N-type substrate (see col. 4, lines 49-51) and an N-type dopant (see col. 5, lines 24-28).

With respect to claims 68 and 76, Chern disclose that the dopant is one of Boron and BF (see col. 3, lines 55-57).

With respect to claims 69 and 70, Chern disclose that the dopant has an implant energy from about 5 to about 25 KeV or less than or equal to about 10 KeV (see col. 3, lines 55-58).

With respect to claims 71, Chern does not disclose the exact concentration, as claimed by Applicant. However, the concentration range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or

upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

6. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HOAI PHAM
PRIMARY EXAMINER